

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	718	716/3.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/10 16:30
L2	46	716/3.ccls. and (verilog or vhdl or hdl) near5 ( "c++" or "c" or "cpp" or "c plus plus" )	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/10 16:31
S1	2457632	(compil\$5 or convert\$3 or conversion or translat\$3 or transform\$5 or ( cross near3 compil\$5 ) or reverse) and (verilog and "c++" or "c" or "cpp" or "c plus plus" )	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 17:58
S2	618	717/136.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 17:57
S3	189	717/137.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 17:57
S4	180	717/138.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 17:58
S5	286	717/139.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 17:58
S6	1495	(compil\$5 or convert\$3 or conversion or translat\$3 or transform\$5 or ( cross near3 compil\$5 ) or reverse) and (verilog and "c++" or "c" or "cpp" or "c plus plus" ) and 717/13?.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 17:58
S7	0	(compil\$5 or convert\$3 or conversion or translat\$3 or transform\$5 or ( cross near3 compil\$5 ) or reverse) and (verilog and "c++" or "c" or "cpp" or "c plus plus" ) and 717/13?.ccls. and "verilog to" near2 ( "c++" or "cpp" or "c plus plus" )	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:00

## EAST Search History

S8	4	(compil\$5 or convert\$3 or conversion or translat\$3 or transform\$5 or ( cross near3 compil\$5 ) or reverse) and (verilog and "c++" or "c" or "cpp" or "c plus plus" ) and 717/13?.cccls. and verilog near3 ( "c++" or "cpp" or "c plus plus" )	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:09
S9	10	(compil\$5 or convert\$3 or conversion or translat\$3 or transform\$5 or ( cross near3 compil\$5 ) or reverse or map\$4 ) and (verilog and "c++" or "c" or "cpp" or "c plus plus" ) and 717/13?.cccls. and (verilog or hdl or rtl or vhdl) near3 ( "c++" or "cpp" or "c plus plus" )	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:20
S10	6	S9 not S8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:10
S11	406	(compil\$5 or convert\$3 or conversion or translat\$3 or transform\$5 or ( cross near3 compil\$5 ) or reverse or map\$4 ) same ( verilog or hdl or rtl or vhdl) same ( "c++" or "cpp" or "c plus plus" )	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:21
S12	176	(compil\$5 or convert\$3 or conversion or translat\$3 or transform\$5 or ( cross near3 compil\$5 ) or reverse or map\$4 ) near5 ( verilog or hdl or rtl or vhdl) same ( "c++" or "cpp" or "c plus plus" )	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:24
S13	65	(compil\$5 or convert\$3 or conversion or translat\$3 or transform\$5 or ( cross near3 compil\$5 ) or reverse or map\$4 ) near5 ( verilog or hdl or rtl or vhdl) near5 ( "c++" or "cpp" or "c plus plus" )	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:23
S14	1	(compil\$5 or convert\$3 or conversion or translat\$3 or transform\$5 or ( cross near3 compil\$5 ) or reverse or map\$4 ) near5 ( verilog or hdl or rtl or vhdl) same ( "c++" or "cpp" or "c plus plus" ) and ( "vbscript" or "visual basic script")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:25
S15	37	(compil\$5 or convert\$3 or conversion or translat\$3 or transform\$5 or ( cross near3 compil\$5 ) or reverse or map\$4 ) near5 ( verilog or hdl or rtl or vhdl) same ( "c++" or "cpp" or "c plus plus" ) and ( macro)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:26

## EAST Search History

S16	136	(compil\$5 or convert\$3 or conversion or translat\$3 or transform\$5 or ( cross near3 compil\$5 ) or reverse or map\$4 ) near5 ( verilog or hdl or rtl or vhdl ) same ( "c++" or "cpp" or "c plus plus" ) and ( "task library" or library or driver or header or interface or api)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:27
S17	64	(compil\$5 or convert\$3 or conversion or translat\$3 or transform\$5 or ( cross near3 compil\$5 ) or reverse or map\$4 ) near5 ( verilog or hdl or rtl or vhdl ) same ( "c++" or "cpp" or "c plus plus" ) and ( "task library" or library or driver or header or interface or api) and ( verilog or hdl or rtl or vhdl) near5 ( "# delay" or "ifdef" or "{" or "}" or (register near3 definition) or assignment or event or switch or "case statement" or concat or concatenation or "#define" or const or constant or (bit near3 access\$3 ) ) and (substitut\$3 or translat\$3 or remov\$3 or convert\$3 or insert\$3 )	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:34
S18	6	("6097212"   "6188975"   "6415420"   "6507947").PN. OR ("6606734").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/03/09 18:53

[Home](#) | [Login](#) | [Logout](#) | [Access](#)


## Welcome United States Patent and Trademark Office

### Search Results

[BROWSE SEARCH](#) [IEEE XPLORE](#) [GUIDE](#)

Results for "((verilog to c )<in>metadata)"

Your search matched 1 of 1516137 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by **Relevance** in **Descending** order.

### » Search Options

[View Session](#)
[History](#)
[New Search](#)

### Modify Search

☐ Check to search only within this results set

### » Key

**IEEE** IEEE

**JNL**

Journal or  
Magazine

**IET**  
**JNL**

IET Journal  
or Magazine

**IEEE**  
**CNF**

IEEE  
Conference  
Proceeding

**IET**  
**CNF**

IET  
Conference  
Proceeding

**IEEE**  
**STD**

IEEE  
Standard

**Display** ☒ Citation ☐ Citation &  
**Format:** Abstract

[Select All](#) [Deselect All](#)

- ☐ 1. **A Verilog to C compiler**  
Greaves, D.J.;  
Rapid System Prototyping, 2000. RSP 2000. Proceedin  
Workshop on  
21-23 June 2000 Page(s):122 - 127  
Digital Object Identifier 10.1109/IWRSP.2000.855208  
AbstractPlus | Full Text: [PDF\(164 KB\)](#) **IEEE CNF**  
Rights and Permissions

[Help](#)

Indexed by  
 Inspec

© Co


[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#)
[Search:](#) ☒ The ACM Digital Library ☐ The Guide


[Feedback](#) [Report a problem](#) [Satisfaction s](#)

Published since January 1995 and Published before January 2004

Found 85

Terms used test bench C hdl

Sort results by

[Save results to a Binder](#)

Try an [Advanced Search](#)

Display results

[Search Tips](#)

Try this search in [The ACM](#)

☐ Open results in a new window

Results 1 - 20 of 85

Result page: [1](#) [2](#) [3](#) [4](#) [5](#) [next](#)

Relevance scale

**1** [Hardware/software co-simulation in a VHDL-based test bench approach](#)

Matthias Bauer, Wolfgang Ecker

June 1997 **Proceedings of the 34th annual conference on Design automation DAC '9**

**Publisher:** ACM Press

Full text available: [pdf\(88.32 KB\)](#) Additional Information: [full citation](#), [abstract](#), [reference citations](#), [index terms](#)

Novel test bench techniques are required to cope with a functional test complexity which is predicted to grow much more strongly than design complexity. Our test bench approach attacks this complexity by using a strong hierarchical architecture, application domain-independent synchronization, reusable modules, and easy incremental extendability based on table-driven techniques. In addition, the integration of VHDL/C co-simulation under the control of the test bench makes it possible to use the hardware ...

**2** [System level design research in an industrial setting \(invited talks\): IP reuse in the system chip era](#)

Warren Savage, John Chilton, Raul Camposano

September 2000 **Proceedings of the 13th international symposium on System synthesis ISSS '00**

**Publisher:** IEEE Computer Society

Full text available: [pdf\(728.70 KB\)](#)

KB)

Additional Information: [full citation](#), [abstract](#), [reference](#)

Intellectual Property (IP) Reuse is one of the keys for System on a Chip (SoC) design productivity improvement. Although IP reuse has been explored both technically and business for many years, only recently systematic approaches based on EDA technology are starting to emerge in the marketplace. This paper gives an introduction to IP creation, conversion and the necessary infrastructure. We address the technical challenges and that a strict quality based design methodology is the co ...

### 3 [Testing: On automatic generation of RTL validation test benches using circuit testing techniques](#)



Indradeep Ghosh, Srivaths Ravi

April 2003 **Proceedings of the 13th ACM Great Lakes symposium on VLSI GLSVI**

**Publisher:** ACM Press

Full text available: [pdf\(145.00 KB\)](#) Additional Information: [full citation](#), [abstract](#), [reference](#), [index terms](#)

In this paper, we examine how good validation test benches can be automatically generated starting from the RTL description of a circuit. We develop our methodology based on extensive experiments performed with several popular benchmarks as well as industrial circuits.

**Keywords:** ATPG, OCCOM, RTL ATPG, RTL testing, branch coverage, code coverage, coverage metrics, design validation, fault coverage, generation, path coverage, small validation, test, test sets, testbench, testing, toggle coverage, universal test sets

### 4 [A framework for object oriented hardware specification, verification, and synthesis](#)



T. Kuhn, T. Oppold, M. Winterholer, W. Rosenstiel, Marc Edwards, Yaron Kashai

June 2001 **Proceedings of the 38th conference on Design automation DAC '01**

**Publisher:** ACM Press

Full text available: [pdf\(222.17 KB\)](#) Additional Information: [full citation](#), [abstract](#), [reference](#), [citations](#), [index terms](#)

We describe two things. First, we present a uniform framework for object oriented specification and verification of hardware. For this purpose the object oriented language is introduced along with a powerful run-time environment that enables the designer to perform the verification task. Second, we present an object oriented synthesis that integrates "e" and its dedicated run-time environment into a framework for specification, verification

and synthesis. The usab ...

**Keywords:** high-level synthesis, object oriented hardware modeling, verification

5 Special Session on Design Paradigms: SystemC: a modeling platform supporting multiple design abstractions



Preeti Ranjan Panda

September 2001 **Proceedings of the 14th international symposium on Systems synthesis**  
ISSS '01

**Publisher:** ACM Press

Full text available: pdf(103.89 KB) Additional Information: [full citation](#), [abstract](#), [reference citations](#), [index terms](#)

SystemC is a C++ based modeling platform supporting design abstractions at the register transfer, behavioral, and system levels. Consisting of a class library and a simulation kernel, the language is an attempt at standardization of a C/C++ design methodology, and is supported by the Open SystemC Initiative (OSCI), a consortium of a wide range of system houses, semiconductor companies, Intellectual property (IP) providers, embedded software developers, and design automation tool vendors. The advantage ...

**Keywords:** C/C++ based design, SystemC, hardware description language, system level design

6 A system-level co-verification environment for ATM hardware design

G. Post, A. Müller, T. Grötter

February 1998 **Proceedings of the conference on Design, automation and test in Europe**  
DATE '98

**Publisher:** IEEE Computer Society

Full text available: pdf(69.33 KB)

[Publisher Site](#)

[Publisher Site](#)

[Publisher Site](#)

Additional Information: [full citation](#), [abstract](#), [reference citations](#), [index terms](#)

Common approaches to hardware implementation of networking components start at the VHDL level and are based on the creation of regression test benches to perform simulation validation of functionality. The time needed to develop test benches has proven to be a significant bottleneck with respect to time-to-market requirements. In this paper, we

describe the coupling of a telecommunication network simulator with a VHDL simulator and a hardware test board. This co-verification approach enables the ...


**Keywords:** co-verification, test bench design and reuse, co-simulation, ATM hardware design, system design methodology, interface modeling

7 Moving towards more effective validation: A comparison of three verification techniques: directed testing, pseudo-random testing and property checking

Mike G. Bartley, Darren Galpin, Tim Blackmore

June 2002 **Proceedings of the 39th conference on Design automation DAC '02**

**Publisher:** ACM Press

Full text available:  pdf(212.50 KB) Additional Information: [full citation](#), [abstract](#), [reference citations](#), [index terms](#)



This paper describes the verification of two versions of a bridge between two on-chip functional models. The verification was performed just as the Infineon Technologies Design Centre in Berlin was introducing pseudo-random testing (using Specman) and property checking (using GateProp) into their verification flows and thus provides a good opportunity to compare these two techniques with the existing strategy of directed testing using VHDL bus functional models.

8 Automatic test bench generation for validation of RT-level descriptions: an industrial experience

F. Corno, M. Sonza Reorda, G. Squillero, A. Manzone, A. Pincetti

January 2000 **Proceedings of the conference on Design, automation and test in Europe DATE '00**

**Publisher:** ACM Press


Full text available:  pdf(200.61 KB)  Additional Information: [full citation](#), [references](#), [citing index terms](#)  
[Publisher](#)  
[Site](#)

9 Simulation-guided property checking based on a multi-valued AR-automata


J. Ruf, D. Hoffmann, T. Kropf, W. Rosenstiel

March 2001 **Proceedings of the conference on Design, automation and test in Europe**





**DATE '01****Publisher:** IEEE PressFull text available:  pdf(135.29 KB) Additional Information: [full citation](#), [references](#), [citing index terms](#)**10** Design Technology for Networked Reconfigurable FPGA Platforms

S. Guccione, D. Verkest, I. Bolsens

March 2002 **Proceedings of the conference on Design, automation and test in Europ****DATE '02****Publisher:** IEEE Computer SocietyFull text available:  pdf(264.20 KB) Additional Information: [full citation](#), [abstract](#), [citing](#)

Future networked appliances should be able to download new services or upgrades from network and execute them locally. This flexibility is typically achieved by processors that download new software over the network, using JAVA technology. This paper demonstrates that FPGAs are a realistic implementation platform for thin server or client applications. FPGAs can offer the same end-user experience as software-based systems, combined with more computational power and lower cost.

**11** New topics in logic synthesis: Verilog HDL, powered by PLI: a suitable framework for describing and modeling asynchronous circuits at all levels of abstraction Arash Saifhashemi, Hossein PedramJune 2003 **Proceedings of the 40th conference on Design automation DAC '03****Publisher:** ACM PressFull text available:  pdf(218.74 KB) Additional Information: [full citation](#), [abstract](#), [reference](#), [index terms](#)

In this paper, we show how to use Verilog HDL along with PLI (Programming Language Interface) to model asynchronous circuits at the behavioral level by implementing CS (Communicating Sequential Processes) language constructs. Channels and communication actions are modeled in Verilog HDL as abstract actions.

**Keywords:** CHP, CSP, PLI, asynchronous circuits, channel, verilog**12** Behavioral synthesis methodology for HDL-based specification and validation

- ◆ D. Knapp, T. Ly, D. MacMillen, R. Miller  
January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation '95**


**Publisher:** ACM Press

Full text available:  pdf(51.94 KB) Additional Information: [full citation](#), [references](#), [citing index terms](#)

**13** IP Design and Reuse: Application of Software design patterns to DSP library design

- ◆ Pontus Åström, Stefan Johansson, Peter Nilsson  
September 2001 **Proceedings of the 14th international symposium on Systems synthesis ISSS '01**

**Publisher:** ACM Press


Full text available:  pdf(144.85 KB) Additional Information: [full citation](#), [abstract](#), [reference citations](#), [index terms](#)

The design of a hardware data path library is one of the harder problems in design for Thanks to the appearance of hardware modeling libraries based on C++, it is possible apply advanced software techniques to design such a library. This paper shows how s design patterns can be applied to hardware design. Design patterns yield a twofold advantage: a faster design process, and a library that is more extensible and modular t equivalent HDL counterpart. From a VHDL-C++ design ...

**14** A C-based synthesis system, Bach, and its application (invited talk)

- ◆ Takashi Kambe, Akihisa Yamada, Koichi Nishida, Kazuhisa Okada, Mitsuhisa Ohnishi, Andrew Kay, Paul Boca, Vince Zammit, Toshio Nomura  
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation ASP-DAC '01**


**Publisher:** ACM Press

Full text available:  pdf(69.87 KB) Additional Information: [full citation](#), [abstract](#), [reference citations](#), [index terms](#)

In system LSI design, a desirable system is one that allows the designer to describe, partition, and verify systems, and to generate circuits efficiently. In this paper, we des C-based system LSI design system called Bach which we have developed. Using the example of an MPEG-4 video codec design, we summarize its design flow, effects an current issues.

**15** Verification of configurable processor cores

◆ Marinés Puig-Medina, Gülbin Ezer, Pavlos Konas


June 2000 **Proceedings of the 37th conference on Design automation DAC '00****Publisher:** ACM PressFull text available:  pdf(79.05 KB) Additional Information: [full citation](#), [abstract](#), [reference citings](#)

This paper presents a verification methodology for configurable processor cores. The simulation-based approach uses directed diagnostics and pseudo-random program gen both of which are tailored to specific processor instances. A configurable and extensib bench serves as the framework for the verification process and offers components nec for the complete SOC verification. Coverage analysis provides an evaluation of how v specific design has been exercised, of the br ...

**Keywords:** co-simulation, configurable processor cores, coverage analysis, design verification, system-on-chip, test generation

**16** Functional test generation for behaviorally sequential models

F. Ferrandi, G. Ferrara, D. Sciuto, A. Fin, F. Fummi

March 2001 **Proceedings of the conference on Design, automation and test in Europe DATE '01****Publisher:** IEEE PressFull text available:  pdf(145.75 KB) Additional Information: [full citation](#), [references](#), [citing index terms](#)**17** Functional verification—real users, real problems, real opportunities (panel)

◆ Jonah McLeod, Nozar Azarakhsh, Glen Ewing, Paul Gingras, Scott Reedstrom, Chris R


June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation D****Publisher:** ACM PressFull text available:  pdf(21.27 KB) Additional Information: [full citation](#), [citing index terms](#)**18** Decomposition of timed decision tables and its use in presynthesis optimizations

Jian Li, Rajesh K. Gupta

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design ICCAD '97**

**Publisher:** IEEE Computer Society

Full text available:  pdf(260.76

KB) 

Publisher

Site

Additional Information: full citation, abstract, reference  
citations, index terms

Presynthesis optimizations transform a behavioral HDL description into an optimized description that results in improved synthesis results. We introduce the decomposition of timed decision tables (TDT), a tabular model of system behavior. The TDT decomposition is based on the kernel extraction algorithm. By experimenting using named benchmarks we demonstrate how TDT decomposition can be used in presynthesis optimizations.


**Keywords:** TDT decomposition, behavioral HDL description, benchmarks, circuit synthesis, decision tables, kernel extraction algorithm, optimized HDL description, presynthesis optimizations, system behavior model, timed decision table decomposition


19 A VHDL-based methodology for the design and verification of pipeline A/D converters

 Eduardo Peralías, Antonio J. Acosta, Adoración Rueda, José L. Huertas

January 2000 **Proceedings of the conference on Design, automation and test in Europe DATE '00**

**Publisher:** ACM Press

Full text available:  pdf(189.55

KB) 

Publisher

Site

Additional Information: full citation, references, citing  
index terms

20 High Level and Architectural Synthesis: Object oriented hardware synthesis and verification

 T. Kuhn, T. Oppold, C. Schulz-Key, M. Winterholer, W. Rosenstiel, M. Edwards, Y. K. Kwon

September 2001 **Proceedings of the 14th international symposium on Systems synthesis ISSS '01**

**Publisher:** ACM Press

Full text available:  pdf(96.62

KB)

Additional Information: full citation, abstract, reference  
citations, index terms

The synthesis of hardware from object oriented specifications is presented. Our approach utilizes the *e* language that has been proven to be highly efficient for the verification of hardware. The *e* language is similar to Java and provides additional constructs for specification and verification of hardware. We describe an automated design flow for synthesis of object oriented descriptions that tightly integrates simulation based verification. The usability of our approach is demonstrated by a case study.





**Keywords:** high-level synthesis, object oriented hardware modeling, verification

Results 1 - 20 of 85

Result page: 1 [2](#) [3](#) [4](#) [5](#) [next](#)

The ACM Portal is published by the Association for Computing Machinery. Copyright © 2007 ACM, Inc.

[Terms of Usage](#) [Privacy Policy](#) [Code of Ethics](#) [Contact Us](#)

Useful downloads:  [Adobe Acrobat](#)  [QuickTime Player](#)  [Windows Media Player](#) 

[Sign in](#)[Google](#)[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [more »](#)[Advanced Search](#)  
[Preferences](#)**Web** Results 1 - 10 of about 116 for **David Greaves + verilog C++**. (0.96 seconds)

### [PPT] Kein Folientitel

File Format: Microsoft Powerpoint - [View as HTML](#)**Verilog -> C. David Greaves**. University of Cambridge ... This is in the class definition and not "static" in C++ mode. 10. © DJ **GREAVES**. VTOC COMPILER ...[www.rsp-workshop.org/History/Slide00/S06P1.ppt](http://www.rsp-workshop.org/History/Slide00/S06P1.ppt) - [Similar pages](#)

### [PDF] Using RTL-to-C++ translation for large soc concurrent engineering ...

File Format: PDF/Adobe Acrobat

by William Stoye, **David Greaves**, Neil Richards and James Green. n this article, we consider the ... VTOC converts synthesisable **Verilog** into C++. It ...[ieeexplore.ieee.org/iel5/8517/26918/01196363.pdf](http://ieeexplore.ieee.org/iel5/8517/26918/01196363.pdf) - [Similar pages](#)

### Tenison EDA's Dr. David Greaves Giving Keynote Address On High ...

Dr. **David Greaves**, chief scientist and founder of Tenison EDA, the industry ... C++, and SystemC modeling 10 times faster than the best compiled **Verilog**, ...[www.findarticles.com/p/articles/mi\\_m0EIN/is\\_2003\\_Sept\\_10/ai\\_107540932](http://www.findarticles.com/p/articles/mi_m0EIN/is_2003_Sept_10/ai_107540932) - 31k - [Cached](#) - [Similar pages](#)

### D J Greaves Publications

Also appeared as: Using RTL-to-C++ translation fro concurrent engineering.

William Stoye, **David Greaves**, Neil Richards, James Green. in IEE Electronic ...[www.cl.cam.ac.uk/~djg11/pubs/pubs.html](http://www.cl.cam.ac.uk/~djg11/pubs/pubs.html) - 7k - [Cached](#) - [Similar pages](#)

### Model Checking a CAN network of PIC CPUs

**David Greaves**, MJ Nam, Univ Cambridge, Computer Laboratory ... The closed

system can be written out as a synthesiable **Verilog** RTL file giving a direct ...  
[www.cl.cam.ac.uk/research/srg/HAN/Lambda/paper.html](http://www.cl.cam.ac.uk/research/srg/HAN/Lambda/paper.html) - 10k -  
[Cached](#) - [Similar pages](#)

## Chip Design Magazine

By Neil Richards, James Green, William Stoye, and **David Greaves** ... U.K.) to convert the synthesizable **Verilog** into C, C++, or SystemC, which provided a ...  
[www.chipdesignmag.com/display.php?articleId=6&issueId=2](http://www.chipdesignmag.com/display.php?articleId=6&issueId=2) - 50k -  
[Cached](#) - [Similar pages](#)

## The Chilli

Tenison EDA was founded in 2000 by Dr. **David Greaves**, who previously co-founded ... of a complete **Verilog** design in the form of a C++/SystemC program. ...  
[www.thechilli.com/articles/markets/high-tech/H014\\_dueDiligenceTenison.asp](http://www.thechilli.com/articles/markets/high-tech/H014_dueDiligenceTenison.asp) - 49k -  
[Cached](#) - [Similar pages](#)

## [PDF] C Models Speed Co-Design

File Format: PDF/Adobe Acrobat - [View as HTML](#)

by Neil Richards, James Green, William Stoye, and **David Greaves** ... the synthesizable **Verilog** into C, C++, or SystemC, which ...  
[www.tenison.com/files/CModelsSpeedCo-Design.pdf](http://www.tenison.com/files/CModelsSpeedCo-Design.pdf) - [Similar pages](#)

## [PDF] Short Report

File Format: PDF/Adobe Acrobat - [View as HTML](#)

Dr **David Greaves** is a lecturer at the University of Cambridge Computer Laboratory, and the founder ... Tenison VTOC models **Verilog** in C, C++, or SystemC. ...  
<https://www.publications.cl.cam.ac.uk/300/01/DesignCon.pdf> - [Similar pages](#)

## EDACafe Weekly : SystemVerilog in the news (again) - October 13, 2003

**David Greaves** is a Professor in the Computer Science Laboratory at Cambridge ... I first heard of **Verilog** when I was at Silicon Graphics back in 1988. ...  
[www10.edacafe.com/nbc/articles/view\\_weekly.php?articleid=209247&page\\_no=4](http://www10.edacafe.com/nbc/articles/view_weekly.php?articleid=209247&page_no=4) - 28k - [Cached](#) - [Similar pages](#)

Result Page:    [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#)    [Next](#)

---

[Search within results](#) | [Language Tools](#) | [Search Tips](#) | [Dissatisfied? Help us improve](#)

---

[Google Home](#) - [Advertising Programs](#) - [Business Solutions](#) - [About Google](#)

©2007 Google